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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
FIEGLE, RYAN PAUL	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/18/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/088,988	NIE, XIAONING	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: "of" on line 14 of claim 1 should be if; "if" should be "is". Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auslander, EPO 0 130 381, in view of Mahlke et al., "A Comparison of Full and Partial Predicated Execution Support for ILP Processors", herein referred to as Mahlke, and in view of Kadosumi et al. (US Patent 5,870,620).

4. As per claim 1, Auslander teaches a method for processing conditional instructions in a processor with pipeline architecture, the method comprising:

a. Loading and decoding a processor the processor instruction containing an instruction opcode (bits 0-6), register addresses (bits 11-16, RA) and a relative jump distance (bits 16-31, D field).

b. And jumping to a jump address as a function of the relative jump distance contained in the processor instruction if the post-condition is fulfilled and the

checked flag bits are set: [Page 33, if the post-condition is fulfilled when the specified bits are checked, the branch is taken, i.e., the PC is updated by adding the D field to the current PC.]

Auslander fails to teach wherein the instruction contains a precondition, which specifies under which conditions the instruction is actually to be executed, and the step of the execution of the decoded processor instruction if the precondition is fulfilled.

However, Mahlke teaches wherein every instruction contains an additional source operand to hold a predicate specifier (precondition) (Page 139, left column, lines 1-3). If the precondition is true, the instruction is executed, however if it is false, the instruction is not executed. (Page 139, right column, 3rd full paragraph). Mahlke also teaches that using the predicated method in place of a large portion of branch instructions (i.e., not all) improves processor performance significantly (Page 139, left column, first full paragraph). It is therefore inherent that there are some unconverted branch instructions that contain a predicate specifier (precondition). Also, a predicated branch instruction is shown in figure 3, under heading 'fully predicated code' and sub-heading 'branch instructions'. Predicating instructions is a well-known method in the art that allows improved processing by not stalling the pipeline while a branch instruction is evaluated. Instead, the instructions that are dependent on the branch instruction contain predicates, and they are executed as normal, except their results are not committed. When the predicate contains a valid value, the instructions from the correct execution path are committed while the other instructions and results are simply ignored. (See 1 Introduction, Mahlke, page 138).

The combination of the full predication of Mahlke and Auslander would result in a branch instruction (conditional jump instruction) with a precondition (predicate specifier) and post-condition (c). It would have been obvious to one of ordinary skill in the art to add the full predication of Mahlke to the instruction processing of Auslander because of the improved processing performance it offers. (Mahlke, page 138, Abstract, final sentence).

Auslander and Mahlke fail to teach a post-condition which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked, wherein the post-condition comprises a plurality of post-condition bits that are checked in the processor and carrying out no-jump if the post-condition is not fulfilled and checking the corresponding flag bits if the post condition is fulfilled.

Kadosumi teaches an instruction that can complete an operation, and if a logic test associated with that instruction is true, checking flag bits within the processor, and if those bits are set accordingly, branching to another instruction. This is completed with only one instruction (Kadosumi: column 13, lines 20-57).

Applying Kadosumi to Auslander and Mahlke would provide the advantage of to being able to complete an operation, a logic test, and a branch all in one instruction. Combined with the predication outlined above in Auslander and Mahlke, this would be able to cut down functions that could take upto 4 or 5 instructions down to merely 1. This is a great benefit. Not only would it significantly cut down on code size, but an improvement in performance would also be expected.

Therefore, it would have been obvious to one of ordinary skill in the pertinent art that applying Kadosumi's instruction post-condition to Auslander and Mahlke would provide the benefit of shorter code and higher performance.

5. As per claim 3, Auslander teaches an apparatus for processing conditional jump instructions in a processor with pipeline computer architecture, the apparatus comprising:

-An instruction decoder (paragraph 3, left column, page 5) for decoding a processor instruction (Branch True or Branch False instruction, page 33) that contains an instruction opcode (bits 0-6), register addresses (bits 11-16, 'RA' field), relative jump distance (bits 16-31, "D" field), and a post-condition, which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked:('bits 6-11, "BI" field): [Page 33]

Auslander fails to teach the processor instruction containing a precondition, which specifies under which conditions the instruction is actually to be executed, and the instruction decoder is operable to check, in the case of a fulfilled precondition, whether the post-condition is fulfilled and, in the case of a fulfilled post-condition, driving a program counter for forming jump address as a function of the relative jump distance contained in the processor instruction.

However, Mahlke teaches wherein every instruction contains an additional source operand to hold a predicate specifier (precondition) (Page 139, left column, lines 1-3). If the precondition is true, the instruction is executed, however if it is false, the instruction is not executed. (Page 139, right column, 3rd full paragraph). Mahlke also

teaches that using the predicated method in place of a large portion of branch instructions (i.e., not all) can improve processor performance significantly (Page 139, left column, first full paragraph). It is therefore inherent that there are some unconverted branch instructions that contain a predicate specifier (precondition). Also, a predicated branch instruction is shown in figure 3, under heading 'fully predicated code' and sub-heading 'branch instructions'. Predicating instructions is a well-known method in the art that allows improved processing by not stalling the pipeline while a branch instruction is evaluated. Instead, the instructions that are dependent on the branch instruction use predicates, and the instructions are executed as normal, except their results are not committed. When the predicate contains a valid value, the instructions from the correct execution path are committed while the other instructions and results are ignored or discarded. (See 1 Introduction, Mahlke, page 138).

The combination of the full predication of Mahlke and Auslander would result in a branch instruction (conditional jump instruction) with a precondition (predicate specifier) and post-condition (BI), wherein the precondition would prevent the conditional jump instruction from being executed if false. It would have been obvious to one of ordinary skill in the art to add the full predication of Mahlke to the instruction processing of Auslander because of the improved processing performance it offers. (Mahlke, page 138, Abstract, final sentence).

Auslander and Mahlke fail to teach wherein the instruction decoder is operable to check, whether the post-condition is fulfilled and the flag bits are set, if positive driving a

program counter for forming a jump address as a function of the relative jump distance contained in the processor instruction.

Kadosumi teaches an instruction that can complete an operation, and if a logic test associated with that instruction is true, checking flag bits within the processor, and if those bits are set accordingly, branching to another instruction. This is completed with only one instruction (Kadosumi: column 13, lines 20-57).

Applying Kadosumi to Auslander and Mahlke would provide the advantage of to being able to complete an operation, a logic test, and a branch all in one instruction. Combined with the predication outlined above in Auslander and Mahlke, this would be able to cut down functions that could take upto 4 or 5 instructions down to merely 1. This is a great benefit. Not only would it significantly cut down on code size, but an improvement in performance would also be expected.

Therefore, it would have been obvious to one of ordinary skill in the pertinent art that applying Kadosumi's instruction post-condition to Auslander and Mahlke would provide the benefit of shorter code and higher performance.

Response to Arguments

6. Applicant's arguments with respect to claims 1 and 3 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan P Fiegle
Examiner
Art Unit 2183

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